Amendments to the Claims

The listing of claims will replace all prior versions, and listings of claims in the application.

1. (Currently Amended) A communication device, comprising:

a master signal generator adapted to generate a master timing signal;

a receive-lane adapted to receive an analog serial data signal and including:

a sampling signal generator adapted to generate multiple time-staggered sampling signals based on the master timing signal, and

multiple data paths each adapted to sample the serial data signal in accordance with a corresponding one of the time-staggered sampling signals, thereby producing multiple time-staggered data sample streams; and

a data demultiplexer module adapted to time-deskew and demultiplex the multiple time-staggered data streams.

2. (Original) The device of claim 1, wherein the serial data signal has a multi-gigabit symbol rate, each of the time-staggered sampling signals, and correspondingly, each of the time-staggered data sample streams, has a data rate below the multi-gigabit symbol rate, the data demultiplexer being adapted to produce a demultiplexed data sample stream representative of the serial data signal having the multi-gigabit symbol rate.

3. (Original) The device of claim 1, wherein the sampling signal generator includes:

a signal set generator adapted to derive a set of reference signals having different predetermined phases based on the master timing signal; and

a phase interpolator module adapted to derive a timing signal having an interpolated phase from the set of reference signals, the sampling signal generator

being adapted to generate the multiple time-staggered sampling signals from the timing signal such that each of the multiple time-staggered sampling signals has an interpolated phase related to the interpolated phase of the timing signal.

4. (Original) The device of claim 1, wherein each of the multiple data paths includes:

a sampler adapted to sample the analog serial data signal in accordance with the corresponding one of the sampling signals; and

a quantizer following the sampler and adapted to quantize analog data samples produced by the sampler.

5. (Original) The device of claim 4, wherein each of the multiple data paths further includes an analog receive equalizer between the sampler and the quantizer.

6. (Original) The device of claim 1, wherein the data demultiplexer module includes:

a time-deskewer adapted to deskew the time-staggered data sample streams in time; and

a demultiplexer following the time-deskewer and adapted to deserialize deskewed data sample streams produced by the time-deskewer.

7. (Original) The device of claim 1, further comprising a transmit-lane adapted to transmit a second analog serial data signal in accordance with the master timing signal.

8. (Currently Amended) A communication device configured to receive multiple serial data signals, comprising:

a master timing generator adapted to generate a master timing signal;

multiple receive-lanes each configured to receive an associated one of the multiple serial data signals, each receive-lane including:

a phase interpolator adapted to produce a sampling signal having an interpolated phase, and

a data path adapted to sample and quantize the associated serial data signal in accordance with the sampling signal; and

an interpolator control module coupled to each receive-lane, the interpolator control module being adapted to cause the phase interpolator in each receive-lane to rotate the interpolated phase of the sampling signal in the receive-lane at a rate corresponding to a frequency offset between the sampling signal and the serial data signal associated with the receive-lane so as to reduce the frequency offset between the sampling signal and the serial data signal.

9. (Original) The system of claim 8, wherein the interpolator control module is adapted to cause the phase interpolator associated with at least one of the receive-lanes to repetitively rotate the interpolated phase of the sampling signal produced by the phase interpolator through a range of phases spanning 360° at the rate corresponding to the frequency offset associated with the at least one receive-lane.

10. (Original) The device of claim 8, wherein the interpolator control module causes the phase interpolator in each receive-lane to rotate each interpolated sampling signal phase independently of the other one or more interpolated sampling signal phases, whereby the interpolated sampling signal phases associated with the receive-lanes are capable of being rotated at different rates relative to one another.

11. (Original) The device of claim 8, wherein the phase interpolator is adapted to produce the sampling signal based on a plurality of local reference signals derived from the master timing signal and in response to a set of phase control signals.

12. (Original) The device of claim 11, wherein the data path in each receive-lane is adapted to produce a stream of data samples, the interpolator control module including multiple frequency estimators each associated with one of the multiple receive-lanes, each frequency estimator being adapted to estimate the frequency offset between the sampling signal and the serial data signal associated

with the same receive-lane as the frequency estimator, based on the associated data stream.

13. (Original) The device of claim 11, wherein each receive-lane includes a reference signal set generator connected to the master oscillator and adapted to derive a plurality of local reference signals having different predetermined phases based on the master timing signal, each phase interpolator being adapted to produce the sampling signal having the interpolated phase based on the plurality of local reference signals.

14. (Original) The device of claim 8, wherein the master timing generator includes a resonant L-C type oscillator.

15. (Original) The device of claim 8, further comprising multiple transmit-lanes each adapted to transmit a serial data signal in accordance with the master timing signal.

16. (Original) The device of claim 8, wherein the phase interpolator includes:

a plurality of reference stages adapted to control individual magnitudes of a plurality of component signals having different phases responsive to a plurality of control signals from the interpolator control module; and

a combining node adapted to combine the plurality of component signals into the interpolated timing signal.

17. (Original) The device of claim 8, wherein the interpolator control module includes, for each receive-lane:

a phase detector coupled to the data path of the associated receive-lane; and

a phase error processor coupled to the phase detector and adapted to estimate the frequency offset between the sampling signal and the serial data signal associated with the receive-lane, the interpolator control module applying a plurality

of phase control signals to the phase interpolator in accordance with the frequency offset estimate to control the interpolated phase of the sampling signal.

18. (Original) The device of claim 17, wherein the interpolator control module further includes, for each receive-lane, a control signal rotator coupled to the phase interpolator, the control signal rotator being adapted to rotate the plurality of control signals applied to the phase interpolator in accordance with the frequency offset estimate to correspondingly rotate the interpolated phase of the sampling signal associated with the receive-lane.

19. (Original) The system of claim 8, wherein the interpolator control module includes a plurality of interpolator control modules each associated with one of the multiple receive-lanes and each adapted to control the phase interpolator associated with the same receive-lane.

20. (Previously Presented) A method in a communication device, comprising:

(a) generating a master timing signal;

(b) generating multiple time-staggered sampling signals based on the master timing signal;

(c) sampling a received, analog serial data signal in accordance with each of the multiple time-staggered sampling signals, thereby producing multiple time-staggered data sample streams;

(d) time-deskewing the multiple time-staggered data streams; and

(e) demultiplexing multiple time-deskewed data streams produced in step (d).

21. (Original) The method of claim 20, wherein the analog serial data signal has a multi-gigabit symbol rate, each of the time-staggered sampling signals, and correspondingly, each of the time-staggered data sample streams, has a data rate below the multi-gigabit symbol rate, step (e) comprising producing a demultiplexed

data sample stream representative of the serial data signal having the multi-gigabit symbol rate.

22. (Original) The method of claim 20, wherein step (b) comprises generating the multiple time-staggered sampling signals such that each of the sampling signals has an interpolated phase.

23. (Original) The method of claim 20, wherein step (b) comprises:

deriving a set of reference signals having different predetermined phases from the master timing signal;

deriving a timing signal having an interpolated phase from the set of reference signals; and

generating the multiple time-staggered sampling signals from the timing signal such that each of the multiple time-staggered sampling signals has an interpolated phase related to the interpolated phase of the timing signal.

24. (Original) The method of claim 20, wherein step (c) comprises:

sampling the analog serial data signal at sample times according to each of the corresponding sampling signals; and

quantizing analog data samples produced by sampling the analog serial data signal to produce digital data samples.

25. (Original) The method of claim 24, wherein step (c) further comprises equalizing the serial data signal between sampling and quantizing the serial data signal.

26. (Original) The method of claim 20, further comprising:

(f) transmitting a second analog serial data signal in accordance with the master timing signal.

27. (Previously Presented) In a communication device configured to receive multiple serial data signals, a method, comprising:

(a) generating a master timing signal;

(b) deriving multiple sampling signals based on the master timing signal, each of the multiple sampling signals being associated with one of the multiple serial data signals, each of the sampling signals having an interpolated phase;

(c) sampling and quantizing each of the multiple serial data signals according to the associated one of the sampling signals; and

(d) rotating the interpolated phase of each sampling signal at a rate corresponding to a frequency offset between the sampling signal and the corresponding serial data signal so as to reduce the frequency offset between the sampling signal and the corresponding serial data signal.

28. (Original) The method of claim 27, wherein step (d) comprises rotating each interpolated sampling signal phase independently of the other one or more interpolated sampling signal phases.

29. (Original) The method of claim 27, wherein step (b) comprises deriving each of the multiple sampling signals based on a plurality of local reference signals derived from the master timing signal and in response to a set of phase control signals.

30. (Original) The method of claim 29, further comprising prior to step (b), for each serial data signal, estimating the frequency offset between the sampling signal and the serial data signal associated with the sampling signal.

31. (Original) The method of claim 29, wherein step (b) further comprises, for each of the sampling signals:

deriving a plurality of local reference signals having different predetermined phases based on the master timing signal; and

deriving the interpolated phase of the sampling signal based on the plurality of local reference signals.

32. (Canceled)

33. (Previously Presented) The device of claim 1, wherein the a master signal generator, the receive-lane, and the data demultiplexer module are implemented on an integrated circuit chip.

34. (Previously Presented) The device of claim 8, wherein the master timing generator, the multiple receive-lanes, and the interpolator control module are implemented on an integrated circuit chip.